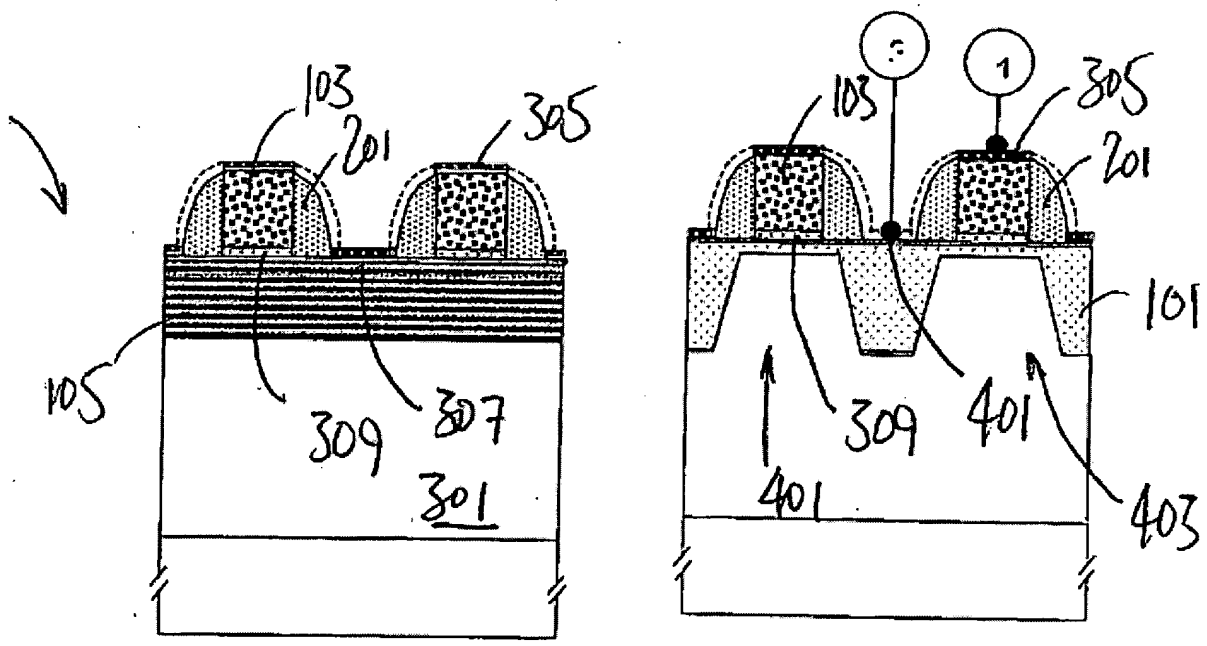
REMARKS/ARGUMENTS

Claim 1 is amended by this response. No claims are canceled or added. Accordingly, claims 1-10 remain pending in the instant application.

As a threshold matter, in the most recent office action the Examiner objected to claim 1 because of certain informalities. Applicants have now amended claim 1 to reference the proper antecedent basis for the claim terms "trench isolation region" and "source/drain regions". In view of these claim amendments, it is respectfully asserted that the Examiner's objections to claim 1 have now been overcome.

Embodiments in accordance with the present invention relate to methods of fabricating memory devices. As shown in Figures 3-4 (reproduced in part, respectively, below), one feature of the claimed embodiments is the formation of gate sidewall spacers (201) to separate a gate (103) from source/drain regions (105) and from a trench isolation region (101):



Accordingly, claim 1 recites as follows:

1. A method for manufacturing ROM memory devices, the method comprising:

. . . forming a first sidewall spacer overlying a first side of the gate structure and a second sidewall spacer overlying a second side of the gate structure, each of the sidewall spacers including the first sidewall spacer and the

> second sidewall spacer being configured to-extend over and overlap a portion of the trench isolation structure and to extend over and overlap a portion of source/drain regions, each of the sidewall spacers including the first sidewall spacer and the second sidewall spacer being adapted to separate the gate structure from the trench isolation region and to separate the gate structure from the source/drain regions . . . . (Emphasis added)

Another feature shown in Figures 3-4 is the formation of silicided regions (305 and 307) overlying the gate structure and the source/drain regions, respectively. Independent claim 1 thus also recites formation of such silicided regions:

> . . . applying a refractory metal layer overlying the gate structure including the first side wall spacer and the second sidewall spacer and exposed portion of the trench isolation structure;
>
> alloying the refractory metal layer to the gate structure and exposed portions of source/drain regions to form silicided regions overlying the gate structure and source/drain regions; and
>
> selectively removing the refractory metal layer from the sidewall spacers and exposed portion of the trench isolation structure. (Emphasis added)

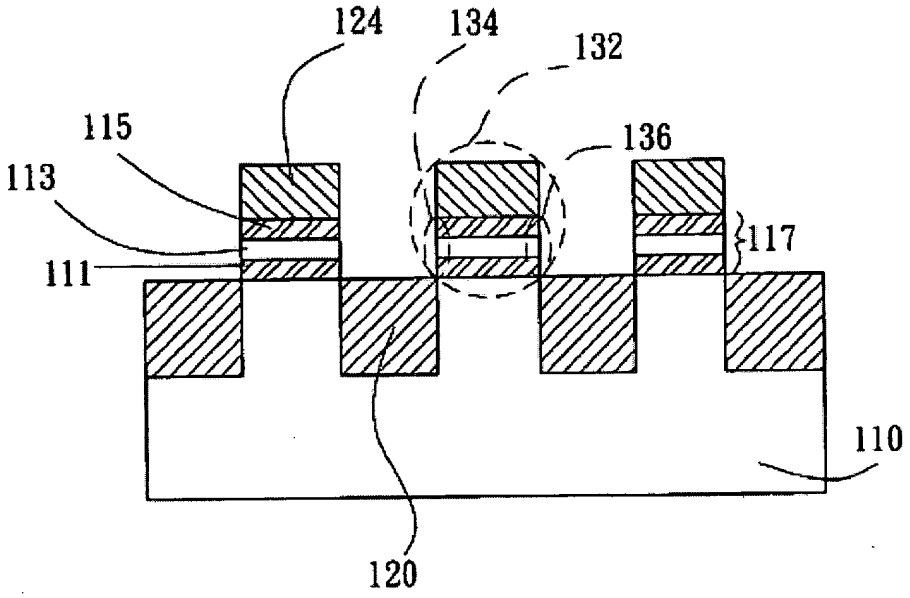
Still another feature shown in Figures 3-4 is the continuous extension of the bit line portion (105) underneath the gate structure (103). Accordingly, independent claim 1 has now been amended to indicate such continuous bit lines:

> forming a trench isolation structure within a cell region of a semiconductor substrate, the cell region being in an array region for ROM memory devices, the trench isolation structure being provided to separate a continuous bit line region of the cell from another continuous bit line region from another cell . . . . (Emphasis added)

The pending claims stand rejected as obvious under 35 U.S.C. 103(a) based upon U.S. Patent Application No. US 2005/006694 A1 to Liu ("the Liu Application"), taken in combination with U.S. Patent No. 6,372,580 B1 to Shiau ("the Shiau Patent"). These obviousness claim rejections are traversed as follows.

The Liu Application is the primary reference relied upon by the Examiner. The Liu Application, however, fails to teach or suggest any the three elements of pending claim 1 discussed specifically above.

For example, nowhere does the Liu Application teach or even suggest formation of a sidewall spacer adapted to separate a gate from source/drain regions. Rather, as explicitly shown and described in connection with FIG. 4D (reproduced below), bit lines (120) are formed by ion implantation directly aligned with the overlying word lines (124) (See ¶**[0034]**):



Moreover, the Liu Application also fails to teach or even suggest the continuous bit line structures that are recited in claim 1. Instead, the Liu Application repeatedly emphasizes the discontinuous nature of the bit lines 120. (See ¶**[0030]**)

Finally, the Liu Application also fails to teach, or even suggest, the silicided regions recited in the claimed embodiments. Rather, as also shown in FIG. 4D, the top surfaces of gate (124) and discontinuous bit lines (120) comprise silicon, rather than silicide. There is absolutely no teaching or suggestion in the Liu Application regarding silicide formation.

In an effort to provide the teaching lacking from the Liu Application, the Examiner has combined that reference with the Shiau Patent. However, the Examiner is respectfully reminded of a key requirement for establishing a prima facie case of obviousness:

> there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. (MPEP 2143).

Such teaching or suggestion to make the claimed combination must be found in the prior art, not in applicant's own disclosure. In re Vaeck, 947 F.2d 488 (Fed.Cir. 1991).

Here, there is absolutely no suggestion in the Liu Application that would motivate one of ordinary skill in the art to combine this reference with the Shiau Patent. Specifically, the Liu Application addresses the problem in the prior art of unwanted diffusion of dopant in buried bit lines resulting from thermal processing steps:

> **[0011]** Because the barrier diffusion oxide 22 and the word lines 24 are completed by thermal process, and also the buried bit lines 20 is formed prior to the formation of the barrier diffusion oxide 22 and the word lines 24, the ion dopant of the buried bit lines 20 tends to diffuse during and after the thermal process. Thereby the concentration of the ion dopant of the buried bit lines 20 differs from the original. The electricity quality of the NOR type N-bit 30 is consequently influenced.

Accordingly, the process flow taught by the Liu Application expressly avoids heat treatment steps following the formation of the buried bit lines. (See **¶[0046]**)

By contrast, in the Shiau Patent heat treatment is necessary to form silicide by alloying a refractory metal with the exposed portion of the source/drain regions or the polysilicon gate. As further shown and described in the Shiau Patent, such heat treatment to form silicides takes place after the buried bit lines have already been formed. The timing of such a heat treatment step is inconsistent with the expressed goal of the Liu Application, namely to avoid thermal diffusion of implanted ions of the buried bit line.

Based at least upon this key difference between the Liu Application and the Shiau Patent, one of ordinary skill in the art would hardly have been motivated to combine these references to arrive at the claimed invention.

Of course, the instant application is replete with teaching regarding formation of silicide after a continuous buried bit line has been formed. However, the Examiner is respectfully reminded that any suggestion to combine references must be found in the prior art, and not be based upon applicants' disclosure:

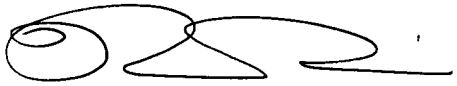
> The tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be

reached on the basis of the facts gleaned from the prior art. (Emphasis added; MPEP 2142)

Here, the Liu Application and the Shiau Patent relied upon by the Examiner differ in important respects, and provide absolutely no motivation for their combination. Resort by the Examiner to Applicants' own disclosure to provide motivation or suggestion for combination is strictly prohibited as impermissible hindsight. And as such, the instant obviousness rejections are improper and should be withdrawn.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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